

Claims

- [c1] A method of forming an ultra thin fully-depleted silicon-on-insulator (SOI) metal oxide semiconductor field effect transistor (MOSFET) structure comprising the steps of: providing a SOI structure comprising a dummy gate that has an upper surface that is coplanar with an upper surface of a planarizing material, said dummy gate is located on a sacrificial oxide that is positioned atop a top Si-containing layer of a SOI substrate; removing the dummy gate to provide a gate opening that exposes a portion of the underlying sacrificial oxide layer, said gate opening defining a device channel in said top Si-containing layer; implanting ions into the device channel, said ions comprise nitrogen or fluorine; removing the sacrificial oxide layer to expose the device channel; recessing the device channel to provide a recessed device channel; and forming the gate, including gate dielectric and gate electrode in said opening atop the recessed device channel.
- [c2] The method of Claim 1 wherein the providing the SOI

structure comprising forming said sacrificial oxide on a surface of said top Si-containing layer; forming a layer of dummy gate material; and patterning said layer of dummy gate material.

[c3] The method of Claim 1 wherein the removing the dummy gate comprises an etching process.

[c4] The method of Claim 3 wherein said etching process comprises chemical downstream etching or KOH etching.

[c5] The method of Claim 1 further comprising forming an outer insulating spacer on the dummy gate prior to forming said planarizing material.

[c6] The method of Claim 1 wherein said implanting said ions is performed at an ion dose from about $1\text{E}13$ to about $5\text{E}14$ atoms/cm².

[c7] The method of Claim 1 wherein said removing the sacrificial oxide comprises a chemical oxide removal (COR) step.

[c8] The method of Claim 7 wherein said COR step comprises a vapor or plasma of HF and NH₃.

[c9] The method of Claim 7 wherein said COR is performed at a pressure of about 6 millitorr or less.

- [c10] The method of Claim 1 wherein said recessing the device channel comprises successive oxidation and COR etching steps.
- [c11] The method of Claim 10 wherein said COR etching comprises a vapor or plasma of HF and NH_3 , said etching is performed at a pressure of about 6 millitorr or less.
- [c12] The method of Claim 1 further comprising etching back said planarizing material.
- [c13] The method of Claim 12 further comprising forming source/drain diffusion regions in said top Si-containing substrate after said etching back step.
- [c14] A silicon-on-insulator (SOI) metal oxide semiconductor field effect transistor (MOSFET) comprising:
a silicon-on-insulator (SOI) substrate having a SOI layer in which a first portion thereof has a thickness of less than about 20 nm;
a gate including a gate dielectric and a gate electrode located atop the first portion of the SOI layer having said thickness; and
source and drain diffusion regions located in a second portion of the SOI layer that is adjacent to said first portion, said second portion of the SOI layer is thicker than the first portion.

- [c15] The SOI MOSFET of Claim 14 further comprising an outer insulating spacer about the gate.
- [c16] The SOI MOSFET of Claim 14 wherein said gate conductor comprises doped polysilicon.
- [c17] The SOI MOSFET of Claim 14 further comprising an undoped or counter-doped device channel beneath said gate, wherein said SOI layer thickness decreases with short channel lengths.
- [c18] The SOI MOSFET of Claim 14 further comprising a doped device channel beneath said gate, wherein said SOI layer thickness increases with short channel lengths.